Figure 1

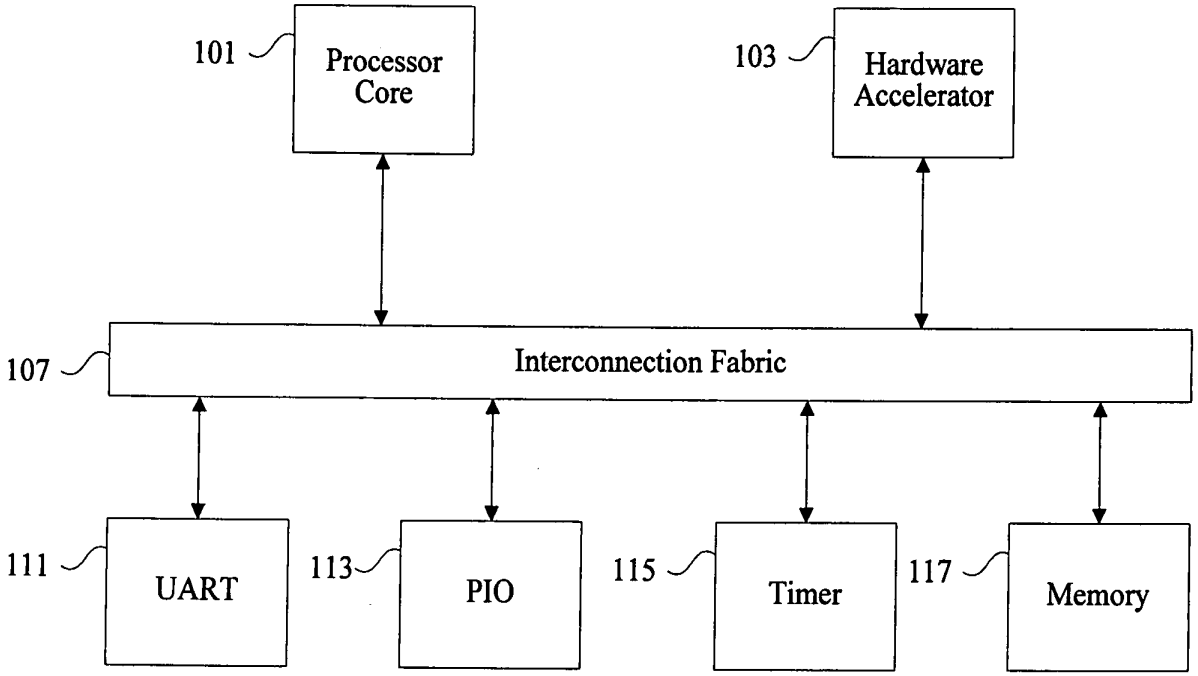

101
Processor Core
103
Hardware Accelerator
107
Interconnection Fabric
111
UART
113
PIO
115
Timer
117
Memory

Figure 2

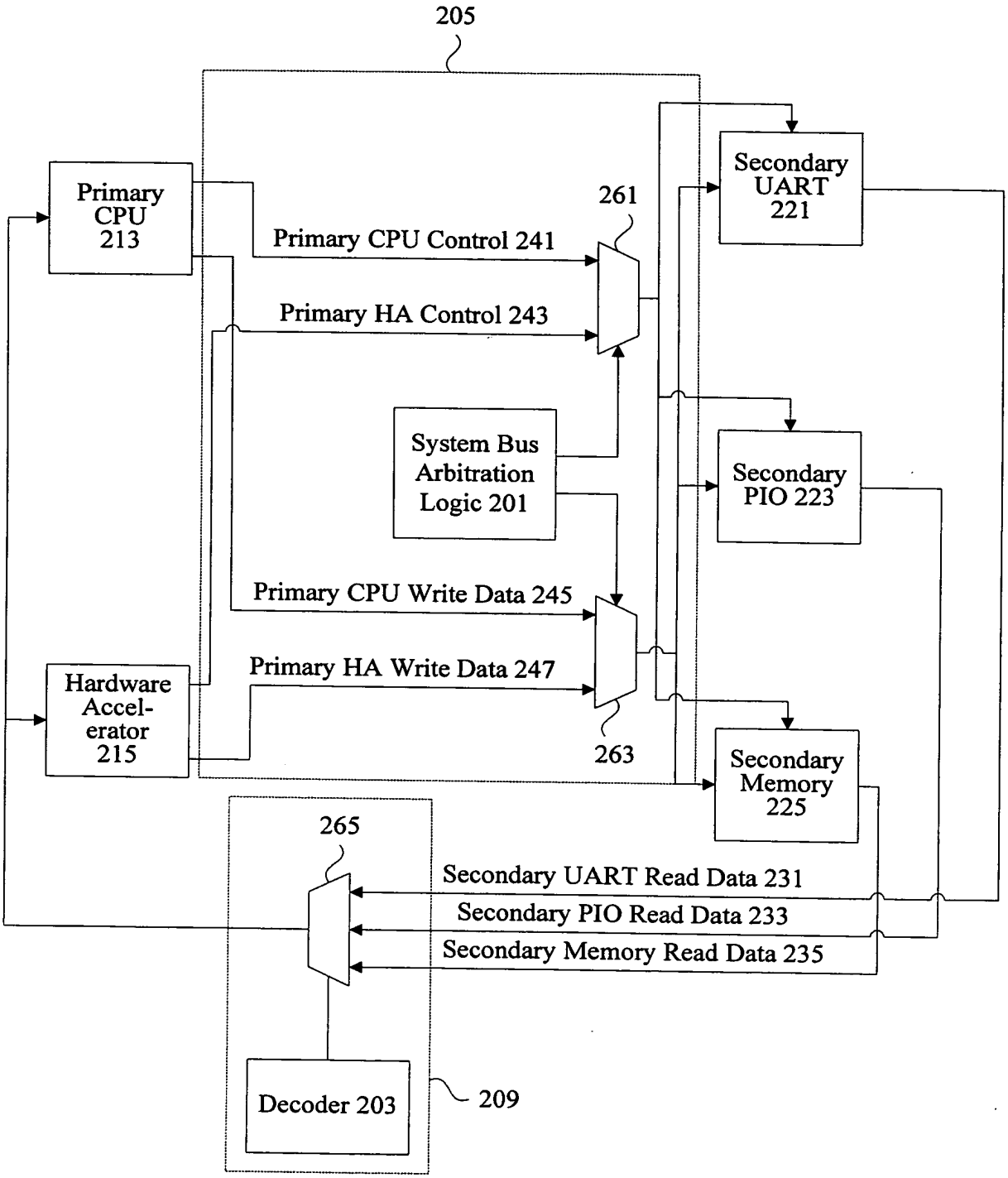

205
Primary CPU 213
Primary CPU Control 241
261
Primary HA Control 243
Secondary UART 221
System Bus Arbitration Logic 201
Secondary PIO 223
Primary CPU Write Data 245
Primary HA Write Data 247
Hardware Accel-erator 215
263
Secondary Memory 225
265
Secondary UART Read Data 231
Secondary PIO Read Data 233
Secondary Memory Read Data 235
Decoder 203
209

Figure 3

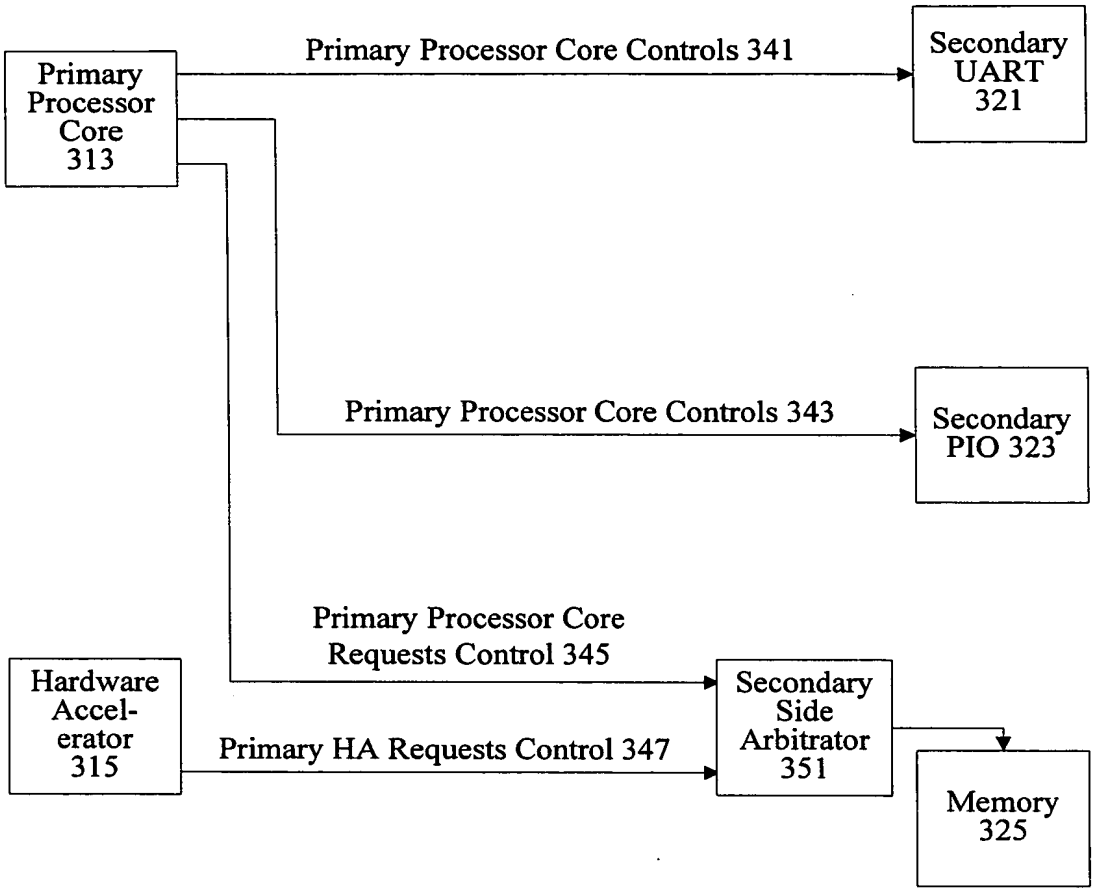

Primary Processor Core 313
Primary Processor Core Controls 341
Secondary UART 321
Primary Processor Core Controls 343
Secondary PIO 323
Primary Processor Core Requests Control 345
Hardware Accel-erator 315
Primary HA Requests Control 347
Secondary Side Arbitrator 351
Memory 325

Figure 4

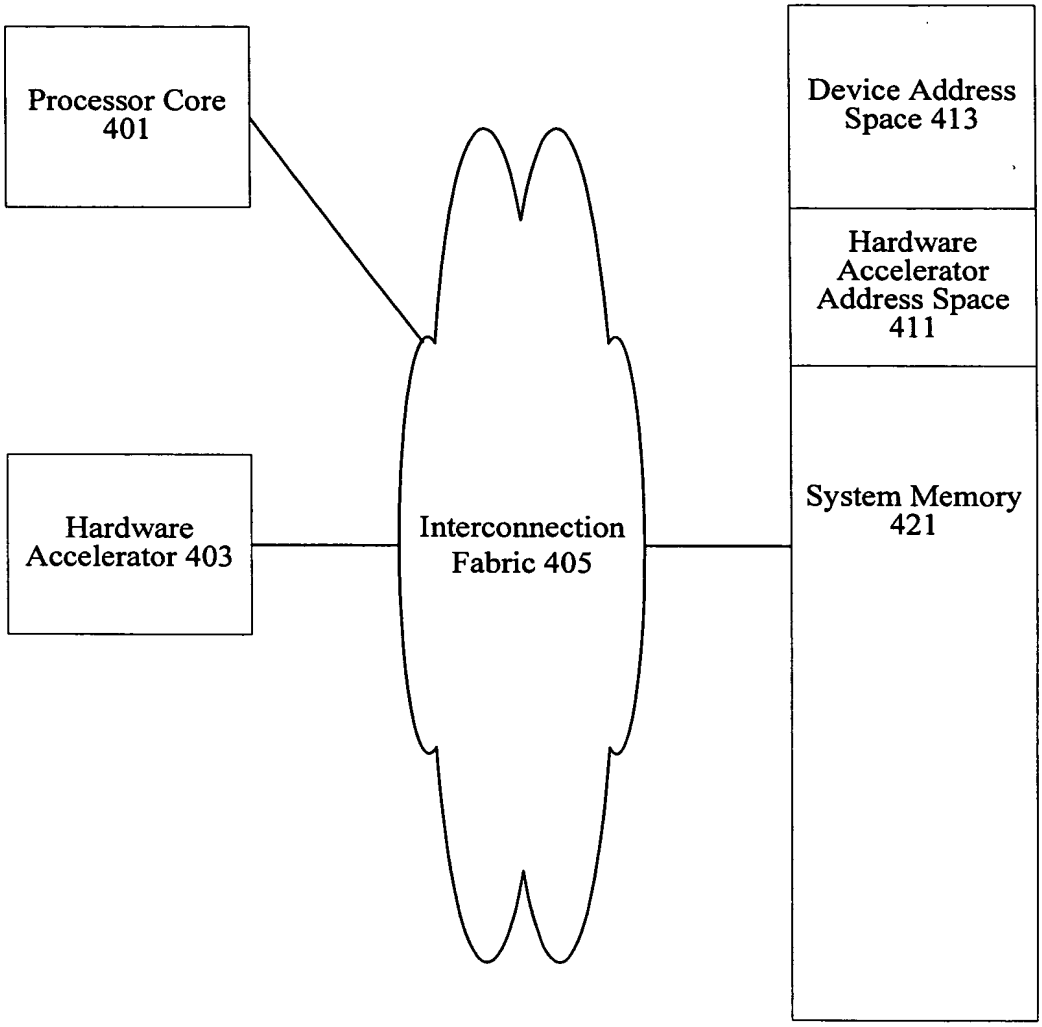

Processor Core
401
Hardware
Accelerator 403
Interconnection
Fabric 405
Device Address
Space 413
Hardware
Accelerator
Address Space
411
System Memory
421

Figure 5

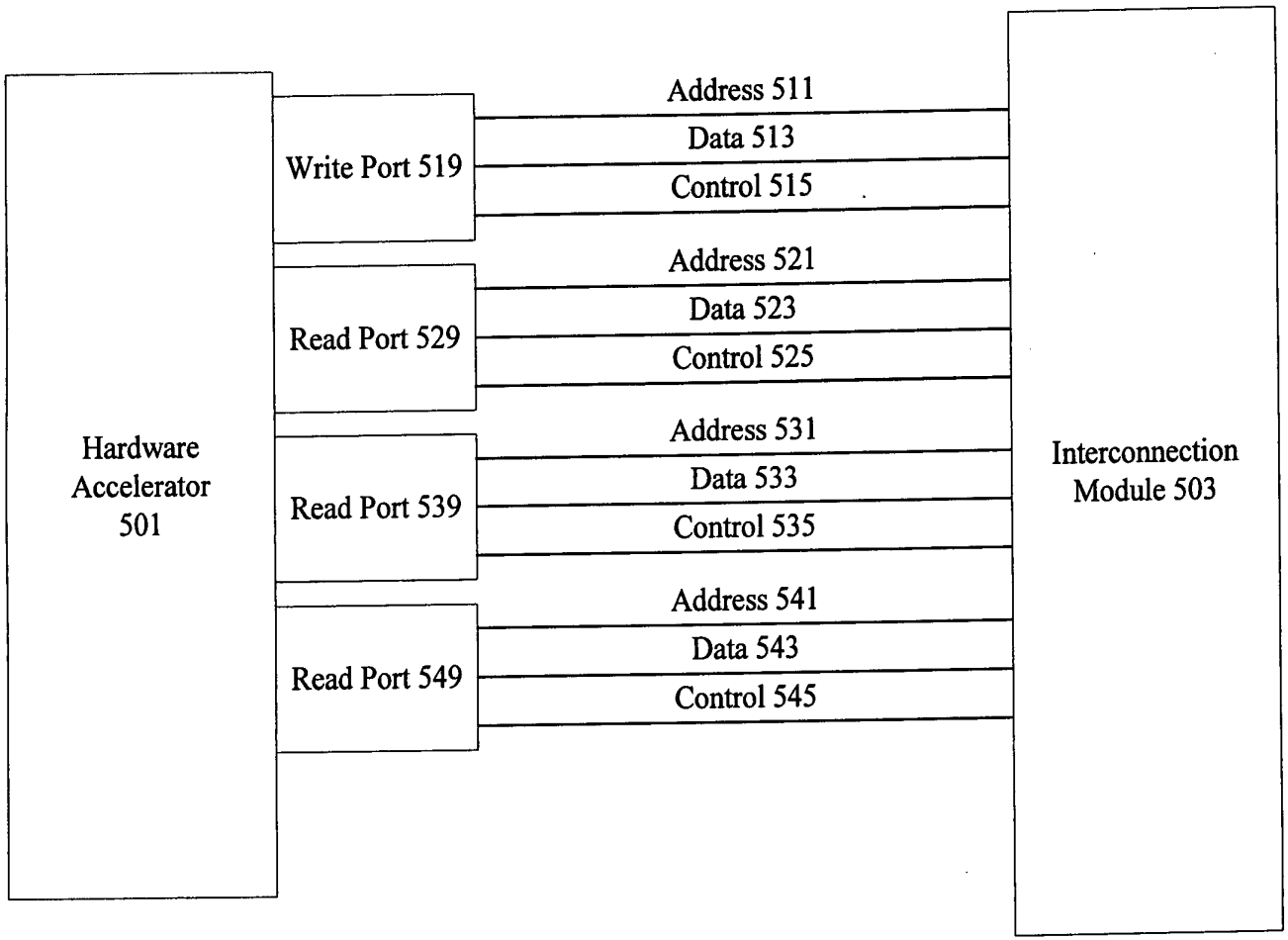
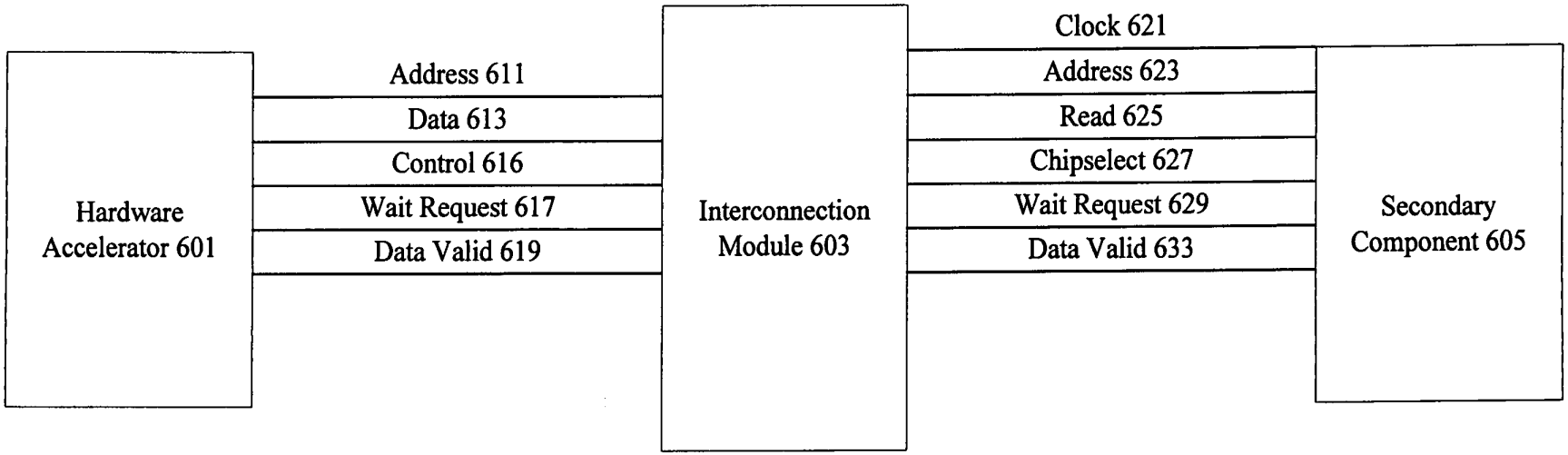

Hardware Accelerator 501
Write Port 519
Read Port 529
Read Port 539
Read Port 549
Address 511
Data 513
Control 515
Address 521
Data 523
Control 525
Address 531
Data 533
Control 535
Address 541
Data 543
Control 545
Interconnection Module 503

Figure 6


Hardware Accelerator 601
Address 611
Data 613
Control 616
Wait Request 617
Data Valid 619
Interconnection Module 603
Clock 621
Address 623
Read 625
Chipselect 627
Wait Request 629
Data Valid 633
Secondary Component 605

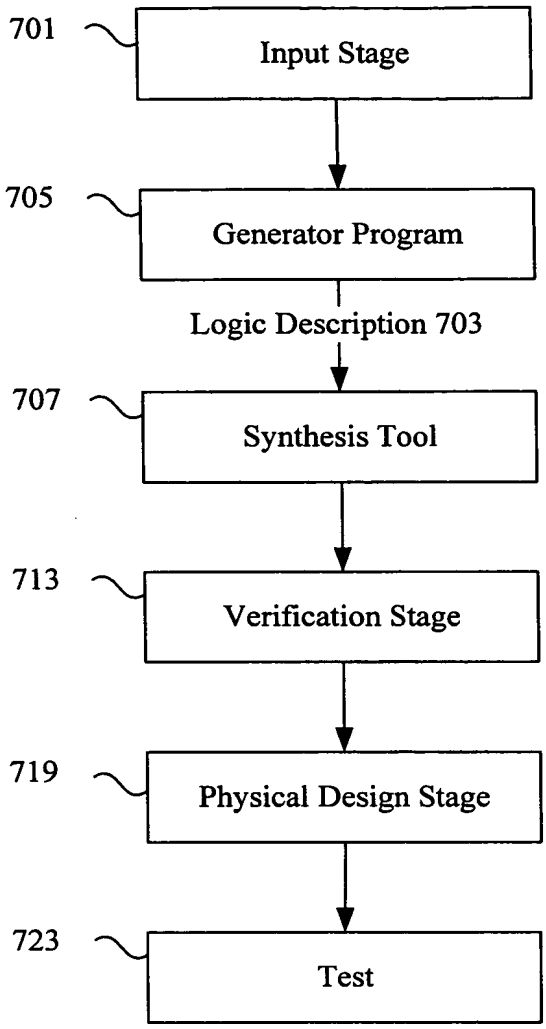

701
Input Stage
705
Generator Program
Logic Description 703
707
Synthesis Tool
713
Verification Stage
719
Physical Design Stage
723
Test

Figure 7

Figure 8

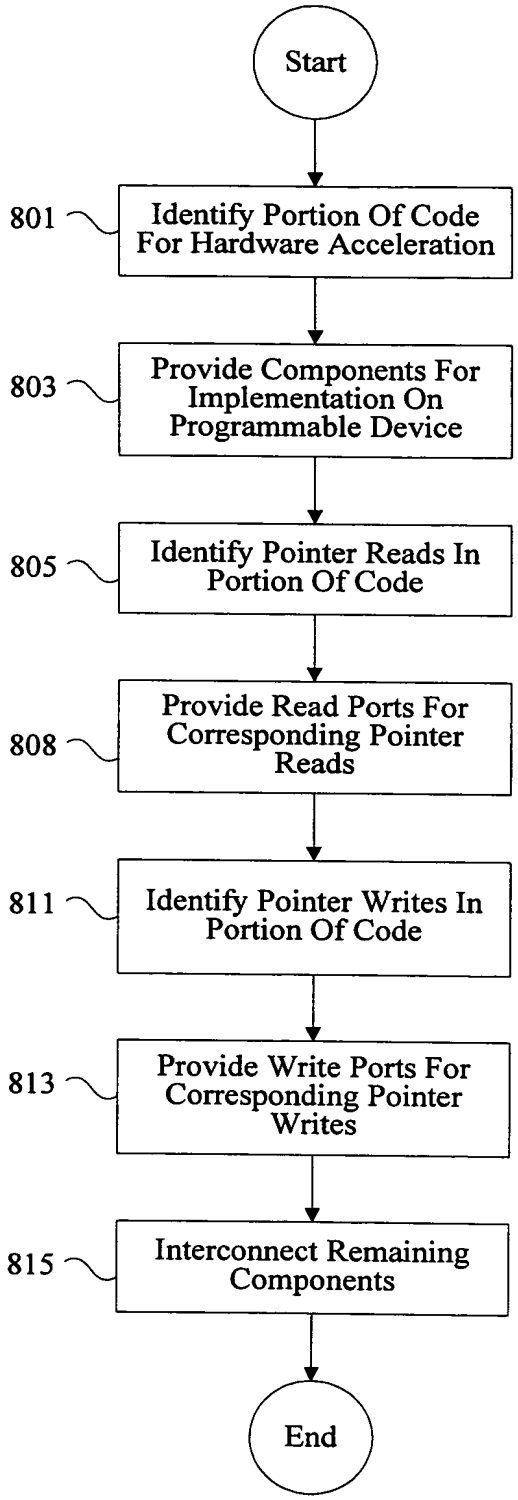
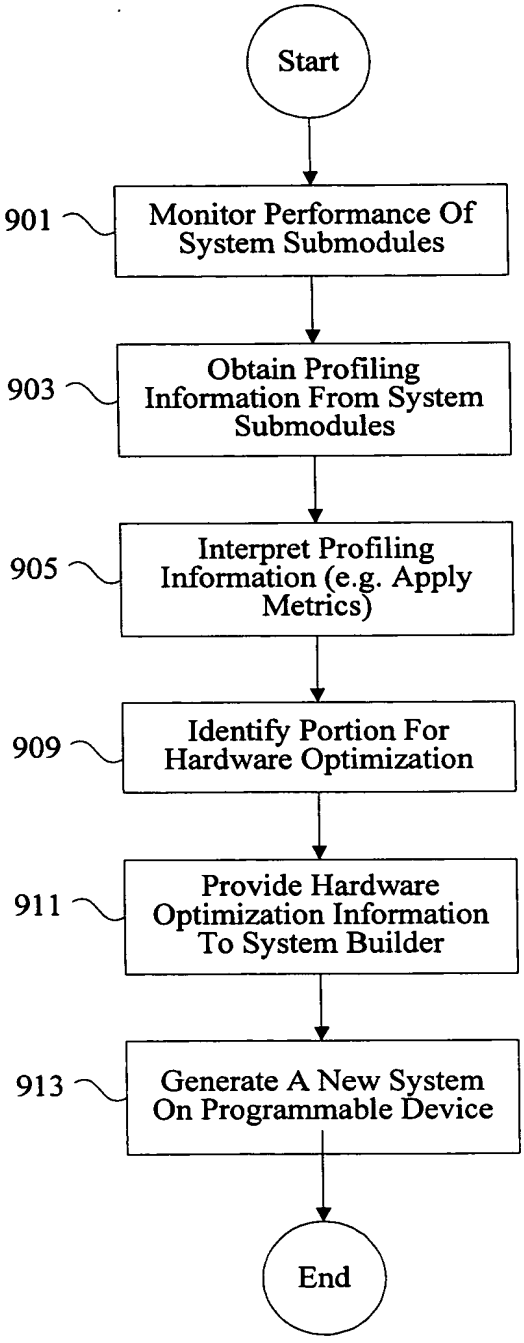

Start
801
Identify Portion Of Code For Hardware Acceleration
803
Provide Components For Implementation On Programmable Device
805
Identify Pointer Reads In Portion Of Code
808
Provide Read Ports For Corresponding Pointer Reads
811
Identify Pointer Writes In Portion Of Code
813
Provide Write Ports For Corresponding Pointer Writes
815
Interconnect Remaining Components
End

Figure 9


Start
901
Monitor Performance Of System Submodules
903
Obtain Profiling Information From System Submodules
905
Interpret Profiling Information (e.g. Apply Metrics)
909
Identify Portion For Hardware Optimization
911
Provide Hardware Optimization Information To System Builder
913
Generate A New System On Programmable Device
End

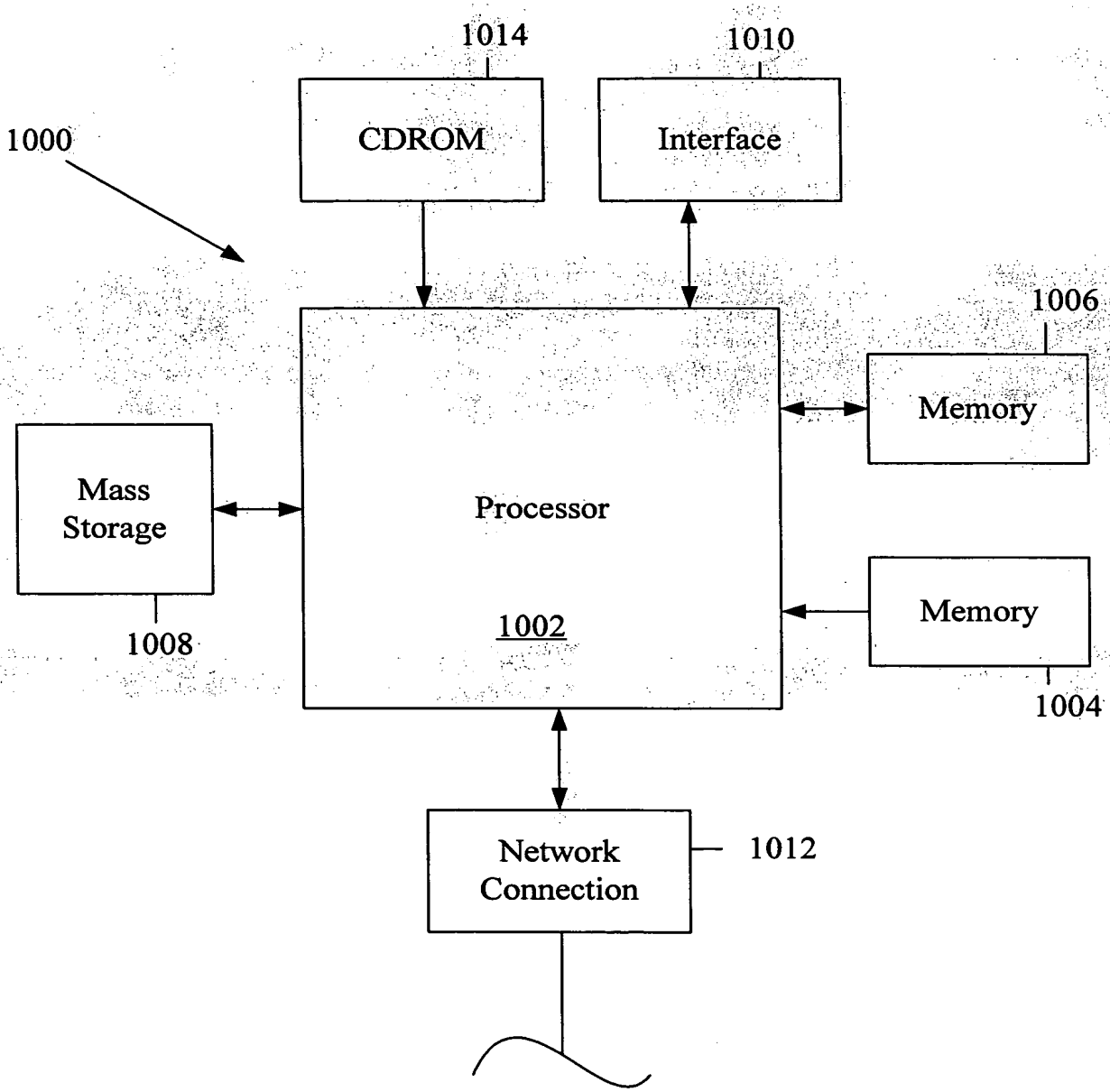

1014
1010
CDROM
Interface
1000
1006
Memory
Mass
Storage
Processor
1002
Memory
1008
1004
Network
Connection
1012

Figure 10